

Confirmation No. 9960

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	MUTH	Examiner:	Zaman, F.
Serial No.:	10/534,164	Group Art Unit:	2111
Filed:	May 5, 2005	Docket No.:	DE02 0252US
Title:	INTEGRATED CIRCUIT WITH LIN-PROTOCOL TRANSMISSION		

REPLY BRIEF

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Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No. 65913

Dear Sir:

This Reply Brief is submitted pursuant to 37 C.F.R. § 41.41(a)(1) for the above-referenced patent application. On November 16, 2007, the Examiner issued an Examiner's Answer to Appellant's Appeal Brief submitted on August 14, 2007, in support of the Notice of Appeal filed on June 14, 2007, and in response to the final rejections of claims 1-6 as set forth in the final Office Action dated March 13, 2007, and further in response to the Advisory Action dated May 7, 2007.

No fee should be required for the timely filing of this Reply Brief. However, if deemed necessary, authorization is given to charge/credit Deposit Account No. 50-0996 (NXPS.206PA) for all required fees/overages.

Status of Claims

Claims 1-6 stand presently rejected and are presented for appeal; a complete listing of the pending claims (and those under appeal) are listed in the attached Claims Appendix, with claim status identifiers.

Grounds of Rejection As Presented In Appeal Brief

1. Claims 1 and 6 stand rejected under 35 U.S.C. § 103(a) over Feuerstraeter *et al.* (U.S. Publ. 2003/0058894) “AAPA” (Applicant’s Admitted Prior Art) and Ishikuri (U.S. 6,674,681).
2. Claims 2 and 3 stand rejected under 35 U.S.C. § 103(a) over Feuerstraeter, AAPA, and Ishikuri as applied to claim 1, and further in view of Bongiorno *et al.* (U.S. 6,292,045).
3. Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) over Feuerstraeter, AAPA and Ishikuri, and further in view of Werle (U.S. 5,778,002).

Appellant's Reply Arguments

All Section 103 rejections must be reversed because the rejections are based upon hindsight motivation including discussion in the Appellant's disclosure, inappropriately assert that a power on clear circuit is a power supply, and involve a modification of the primary (AAPA) reference that would undermine its purpose. In the more detailed discussion below, Appellant fully incorporates the arguments made in the Appeal Brief filed on August 14, 2007 here with the bulk of these arguments omitted for brevity. The following discussion is focused to the issues above and the Response to Arguments in the Examiner's Answer.

The Section 103(a) rejections of claims 1 - 6 must be reversed because the Examiner's proposed motivation is unsupported in and contrary to the cited art, and is improperly based upon the Appellant's disclosure.

The motivation for modifying AAPA with Feuerstraeter as alleged by the Examiner in the Final Office Action, as well as the new allegations of motivation as set forth in the Examiner's Answer, are unsupported by any reference and further contrary to the cited references and understood teachings in the art. In the Final Office Action, the Examiner's asserted motivation relies upon a clearly inaccurate premise that there is motivation to modify AAPA because it could not otherwise communicate. This is contrary to the cited art in that the devices referred to in the cited AAPA reference communicate with different protocols. That is, as is described in detail in the Appeal Brief, absent Feuerstraeter's teachings, the devices in the AAPA *would* communicate with each other and thus the alleged motivation is inapplicable. As is consistent with recent law, a person of ordinary skill in the art having common sense at the time of the invention would not have reasonably looked to Feuerstraeter to solve a problem already solved by AAPA as relevant to devices communicating with each other. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007).

In reply to Appellant's arguments, the Examiner's Answer alleged new motivation, suggesting that Feuerstraeter would "eliminate the need for dedicated external microcontroller to be used to convert ... between protocols." This proposed "motivation" appears to be taken directly from the Appellant's disclosure, which describes example embodiments directed to "an integrated circuit that is suitable for general-purpose use and is capable of performing the

functions described above as a self-contained unit, i.e., with no external microcontroller” (see paragraph 0006). In this regard, the Examiner has yet to provide evidence of motivation from the prior art.

As discussed in the Appeal Brief, the Examiner’s rationale behind different attempts at combining elements has shifted in different Office Actions of record, and has now again shifted in the Examiner’s Answer, which now draws directly from Appellant’s disclosure. Appellant submits that it is clear that the Examiner has used Appellant’s invention to select and combine the elements using improper hindsight reconstruction. For example, in the Office Action of November 15, 2006, the Examiner asserted a first combination of elements that failed to view the invention as a whole and was inconsistent with the teachings of the cited references (see Appellant’s Response of February 9, 2007). In the following Final Office Action of March 13, 2007, the Examiner presented a new combination that, while relying generally on the same references, was configured in a new manner and accompanied with yet another supposed rationale for combining the references. As the record shows and as discussed in the Appeal Brief, this rationale once again improperly ignored the invention as a whole. Appellant submits that the shifting explanations and combinations, together with the newly-alleged motivation drawn directly from Appellant’s disclosure, demonstrate that the Examiner has improperly used the Appellant’s specification as the basis for the current combination of elements. As is consistent with *KSR Int’l Co. v. Teleflex Inc.* cited above, the Examiner should be aware “of the distortion caused by hindsight bias and must be cautious of argument reliant upon ex post reasoning” including, in this instance, using Appellant’s disclosure as alleged motivation.

In short, Examiner has failed to present motivation that is evidenced in the prior art and (accordingly) that suggests that the proposed combination be made or could function. In drawing alleged motivation directly from the Appellant’s disclosure, the Examiner’s Answer also fails to provide any motivation that is evidenced in the prior art. In this regard, there is no reason to combine the references as suggested and the Section 103 rejections, all of which rely upon the proposed combination of Feuerstraeter, AAPA and Ishikuri, must therefore be reversed.

The Section 103 rejections must be reversed because the Examiner is inappropriately asserting Ishikuri's power on clear circuit as an on-chip power supply.

All of the rejections rely upon the Ishikuri reference and its power on clear (POC) circuit as providing correspondence to the claimed system voltage supply. However, as applicable to all of the rejections, the Examiner is confusing the use of an external power source by a system power supply with the system power supply itself. That is, all circuits generally use some sort of external power source (*i.e.*, they do not generate their own electricity), and a separate system power supply that uses the external power source to generate power that is actually used by the circuit. In this instance, Ishikuri's receipt of a system voltage from an external power supply (and control of its application via its POC circuit) simply does not provide teaching or suggestion of the claimed on-chip system voltage supply. The Examiner implicitly acknowledges that "Ishikuri is clearly receiving a system voltage supply" at page 10 of the Examiner's Answer, which is consistent with the above. Accordingly, Ishikuri's POC circuit 1 does not correspond to the claimed system voltage supply and the Section 103(a) rejections of claims 1 and 6 are improper and must be reversed.

The Section 103 rejections must be reversed because the proposed combination of references would undermine the purpose of the primary reference (AAPA).

The record shows that the asserted combination of Feuerstraeter with AAPA would not function properly in a LIN protocol environment. More specifically, the asserted combination would not be capable of receiving and transmitting information using the LIN protocol as in AAPA. For the proposed combination to function, the LAN and WAN-based circuits (*i.e.*, TCP/IP Ethernet protocols) in the cited Feuerstraeter reference would need to function using a LIN protocol or otherwise correspond to the claimed limitations. However, a receiver designed for TCP/IP WAN/LAN protocols cannot be simply substituted into an environment that uses a LIN protocol. There is no explanation in the Feuerstraeter reference or any cited reference that shows how the proposed combination would or could correspond to the claimed limitations (*e.g.*, no portion of the Feuerstraeter reference mentions the LIN protocol or describes any aspect of

the indicated system that could operate with protocols other than WAN or LAN protocols). Consistent with MPEP § 2143.01 and *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984), a §103 obvious-type rejection cannot be maintained when the asserted modification undermines the purpose of the primary reference (a LIN protocol receiver as asserted here). Accordingly, the Section 103(a) rejections of claims 1 and 6 are improper and must be reversed.

VIII. Conclusion

The Section 103 rejections must be reversed because the various rationales alleged as motivation are either inapplicable to the proposed combination of references or draw directly from the Appellant's disclosure. The Section 103 rejections must also be reversed because the proposed modification of the primary AAPA reference would undermine its purpose. The Section 103 rejections must further be reversed because the cited references fail to teach or suggest all of the claimed limitations.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

Respectfully Submitted,

By: 

Name: Robert J. Crawford

Reg. No.: 32,122

Tel: 651 686-6633 ext. 2300

(NXPS.206PA)

CLAIMS APPENDIX
(S/N 10/534,164)

1. (Previously Presented) An integrated circuit having a system base chip that has basic functions for a transmitting and/or receiving system for a vehicle data bus, namely at least a system voltage supply, a system reset and a monitoring function,

an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol, and in particular the LIN (Local Interconnect Network) protocol, that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte,

a serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit.

2. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that there is provided in the integrated circuit an R/C oscillator that acts as a clock-signal source and as a timebase for the bit-rate detection.

3. (Previously Presented) An integrated circuit as claimed in claim 2, characterized in that the clock signal generated by the R/C oscillator may also be provided to circuits outside the integrated circuit, and in particular to a microprocessor.

4. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that the interface circuit may also pass on complete messages.

5. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that the interface circuit performs buffer-storage of data received or to be transmitted.

6. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that the serial/parallel converter converts serial data conforming to the SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface standard into parallel data, or vice versa.